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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/819,883	03/28/2001	Finbarr Denis Long	SRT-022	1043

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EXAMINER	
MANOSKEY, JOSEPH D	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,883	LONG ET AL.	
	Examiner	Art Unit	
	Joseph Manoskey	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7-15 and 19-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-15 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____. .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1-4, 7-15 and 19-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Dhong et al, U.S. Patent 6,772,368, hereinafter referred to as "Dhong".

3. Referring to claim 1, Dhong teaches a pair of processors that both execute the same instruction stream, this is interpreted as a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously (See Fig. 3 and Col. 2, lines 10-20). Dhong also teaches the processors connected to a bus interface unit and arbitration logic, this is interpreted as an I/O node in communication with at least one of the plurality of data processing elements and a switching fabric communicating transactions asynchronously between at least one of the plurality of data processing elements and the I/O node (See Fig. 3 and Col. 3, lines 1-14).

4. Referring to claim 2, Dhong discloses the processors working in lockstep, this is interpreted as the plurality of data processing elements execute the same instruction in lock-step synchronization (See Col. 3, lines 8-10).

5. Referring to claims 3 and 4, Dhong teaches the system being comprised of a dual processor CPU, this is interpreted as each of the plurality of data processing elements comprises a central processing unit and the wherein the CPU further comprises a plurality of processors (See Fig. 3 and Col. 2, lines 10-20).

6. Referring to claim 7, Dhong discloses a bus interface unit, this is interpreted as a channel adapter interconnects the I/O node to the switching fabric (See Fig. 3 and Col. 3, lines 1-14).

7. Referring to claim 8, Dhong teaches both of the dual processors having bus logic for the bus interface unit, this is interpreted as a plurality of channel adapters interconnect, respectively, each of the plurality of data processing elements to the switching fabric (See Fig. 3 and Col. 3, lines 1-14).

8. Referring to claim 9, Dhong discloses the use of a compare unit and signal generators for the dual processors, this is interpreted as a plurality of voter delay buffers wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements (See Fig. 3 and Col. 2, lines 35-50).

9. Referring to claim 10, Dhong teaches the system connected to a bus and memory via a bus interface unit, this is interpreted as a plurality of direct memory access engines in communication with the switching fabric (See Fig. 3 and Col. 3, lines 1-14).

10. Referring to claims 11 and 12, Dhong discloses the system having bus logic for each processor and arbitration logic in the bus interface unit, this is interpreted as plurality of processing elements are identified by a node address and the each of the plurality of data processing elements is individually identified by a respective device address (See Fig. 3 and Col. 3, lines 1-14).

11. Referring to claim 13, Dhong teaches the system being connected to a bus through a bus interface unit for passing information, this is interpreted as the transaction comprises at least one information packet (See Fig. 3 and Col. 3, lines 1-14).

12. Referring to claim 14, Dhong discloses a method for controlling a pair of processors that both execute the same instruction stream, this is interpreted as generating, by a plurality of data elements, identical transactions each having an I/O node address (See Fig. 3 and Col. 2, lines 10-20). Dhong also teaches the processors connected to a bus interface unit and arbitration logic, this is interpreted as

communicating the identical transactions asynchronously on a switching fabric to the I/O node-identified by the I/O node-address (See Fig. 3 and Col. 3, lines 1-14).

13. Referring to claim 15, Dhong discloses the use of a compare unit and signal generators for the dual processors, this is interpreted as communicating identical transaction to a voting unit and transmitting by the voting unit a single transaction asynchronously on a switching fabric (See Fig. 3 and Col. 2, lines 35-50).

14. Referring to claim 19, Dhong discloses a bus interface unit to connect to I/O device and both of the dual processors having bus logic for the bus interface unit, this is interpreted as communicating each of identical transactions from each of the plurality of data processing elements to each of the plurality of channel adapters to the switching fabric, communicating each of the identical transactions from each the plurality of channel adapters to the switching fabric, communicating the identical transactions from the switching fabric to a channel adapter, and communicating the identical transaction from the channel adapter to the I/O node (See Fig. 3 and Col. 3, lines 1-14).

15. Referring to claim 20, Dhong teaches a system containing a pair of processors that both execute the same instruction stream, this is interpreted a plurality of data processing elements executing substantially identical instruction streams substantially simultaneously (See Fig. 3 and Col. 2, lines 10-20). Dhong discloses the use of a compare unit and signal generators for the dual processors, this is interpreted as a

voting module in communication with the plurality of data processing elements for comparing the I/O instructions associated with at least two of the plurality of data processing elements (See Fig. 3 and Col. 2, lines 35-50).

Dhong also teaches the processors connected to a bus interface unit and arbitration logic, this is interpreted as an I/O node in communication with the voting module and a switching fabric communicating transactions asynchronously between the voting module and the I/O node (See Fig. 3 and Col. 3, lines 1-14).

16. Referring to claim 21, Dhong discloses the processors working in lockstep, this is interpreted as the plurality of data processing elements execute the same instruction in lock-step synchronization (See Col. 3, lines 8-10).

17. Referring to claims 22 and 23, Dhong teaches both of the dual processors having bus logic for the bus interface unit, this is interpreted as a channel adapter interconnects the I/O node to a switching fabric and at least one channel adapter interconnects the voting module and the switching fabric (See Fig. 3 and Col. 3, lines 1-14).

18. Referring to claim 24, Dhong discloses the use of a compare unit and signal generators for the dual processors, this is interpreted as a plurality of channel adapters interconnect respectively, each of the plurality of data processing elements to the voting module and wherein the voting module compares packets being communicated from

the channel adapters associated with at least two of the plurality of data processing elements (See Fig. 3 and Col. 2, lines 35-50).

19. Referring to claim 25, Dhong discloses the use of a compare unit and signal generators for the dual processors, this is interpreted as a plurality of voter delay buffers wherein each of the plurality of voter delay buffers is in communication with at least one of the plurality of data processing elements (See Fig. 3 and Col. 2, lines 35-50).

20. Referring to claim 26, Dhong teaches the system being connected to a bus through a bus interface unit for passing information, this is interpreted as the transaction comprises at least one information packet (See Fig. 3 and Col. 3, lines 1-14).

Response to Arguments

21. Applicant's arguments, see page 6 of amendment, filed 10 November 2004, with respect to claim24 have been fully considered and are persuasive. The 35 U.S.C. 112(2) of claim 24 has been withdrawn.

22. Applicant's arguments, see pages 6-13 of amendment, filed 10 November 2004, with respect to the rejection(s)of claim(s) 1-4, 7-15, and 19-26 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Dhong (See above rejection).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JDM
February 25, 2005

DIEU-MINH LE
PRIMARY EXAMINER